A Low Power GaAs Front-end IC with Current-Reuse Configuration Using 0.15 μm Gate MODFETs

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Abstract

We have developed a novel current-reuse configuration of front-end IC, where the current can be reused in the whole circuit blocks such as low noise amplifier, local amplifier and mixer. The power dissipation is reduced by the factor of three. Excellent high frequency performance such as conversion gain of 30 dB and NF of 1.6 dB at 1.5 GHz is attained under the conditions of supply voltage and current of 3.6V and 3mA, respectively.

Introduction

GaAs front-end ICs come to be widely used for mobile communication sets due to their superior RF performance to Si ones. The essential characteristics of those front-end ICs are low noise, high gain, and low consumption power [1-3], which have been attained by the shortening the gate length of GaAs FETs. Although shortening the gate length improves those performance, operation voltage has to be reduced due to the lowered breakdown voltage. It is noted that the typical operation voltage of GaAs FET with 0.15 μm gate-length is less than 1.5V.

Based on this inherent characteristics of the deep submicron GaAs FET, we propose a novel current-reuse configuration of front-end IC, where the LNA (Low Noise Amplifier), the local amplifier and the mixer can reuse the same current.

The performance of the experimentally fabricated IC showed conversion gain of 30.5 dB, noise figure of 1.6 dB, and OIP3 (third-order output intercept point) of 9 dBm at the frequency of 1.5 GHz under the conditions of supplying voltage and current of 3.6V and 3 mA, respectively. This power dissipation of 10.8 mW is the lowest value among those ever reported.

Circuit Design

Figure 1 shows the concept of this current-reuse configuration of the front-end IC. Supplying voltage divided by the number of stages is available for each FET. As mentioned above, supplying voltage can be reduced by employing the deep submicron gate GaAs FETs. Thereby, the power dissipation is reduced by the factor of three compared to the conventional one since the current is reused in the stacked configuration.

Figure 2 shows the schematic circuit of the present IC using the stack configuration. The DC current flows via external choke coils. The source voltages of those FETs are simply determined by gate-biasing voltages keeping the current matching condition. In order to obtain the RF grounds for the source terminals of those FETs, large on-chip bypass capacitors are integrated by using the novel Strontium-Titanium-Oxide (STO) process. It is also noted that all the coupling capacitors connected between those stages also employ the STO capacitor process.

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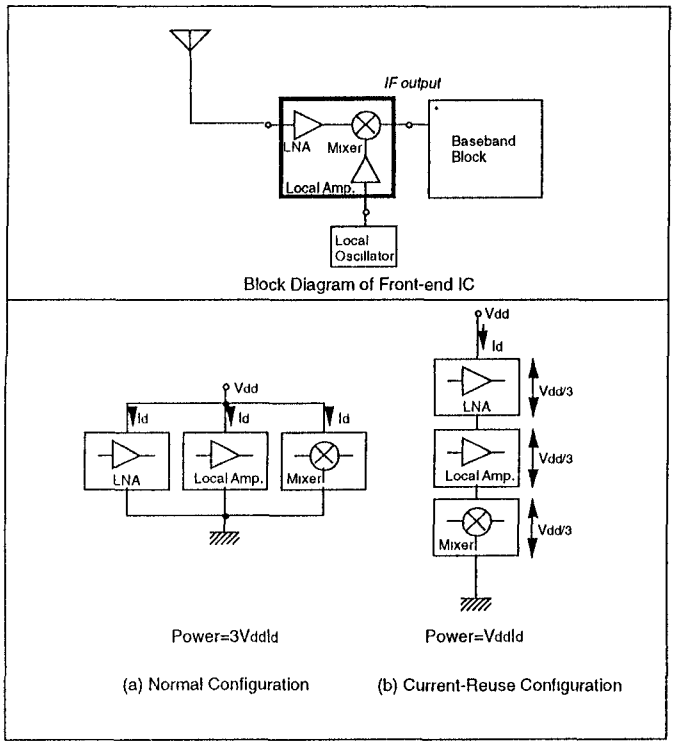

Fig.1 The concept of power reduction by the current-reuse configration.

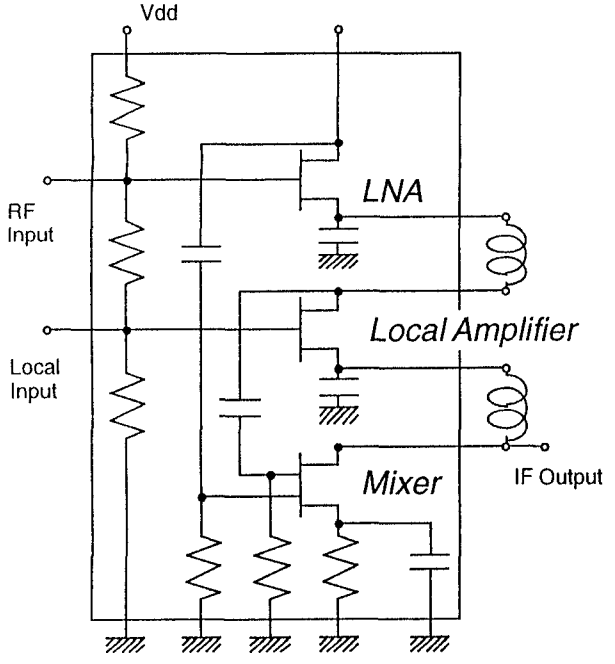

Fig.2 The schematic circuit of the present IC with current-reuse configuration.

Fabrication Process

0.15 μm gate MODFETs were fabricated by using PEL (Phaseshifter-Edge-Line) phase-shift lithography employing a conventional i-line stepper. This PEL process is the most cost-effective fabrication process to obtain the deep submicron FETs [4-5]. The starting material is delta-doped epitaxial wafer grown by MOCVD. The used metals for gate and ohmic electrodes are Ti/Al and AuGeNi, respectively. Figure 3 shows the cross-sectional SEM photographs of 0.15 μm PEL pattern (top figure), and completed GaAs MODFET with T-shaped gate (bottom figure).

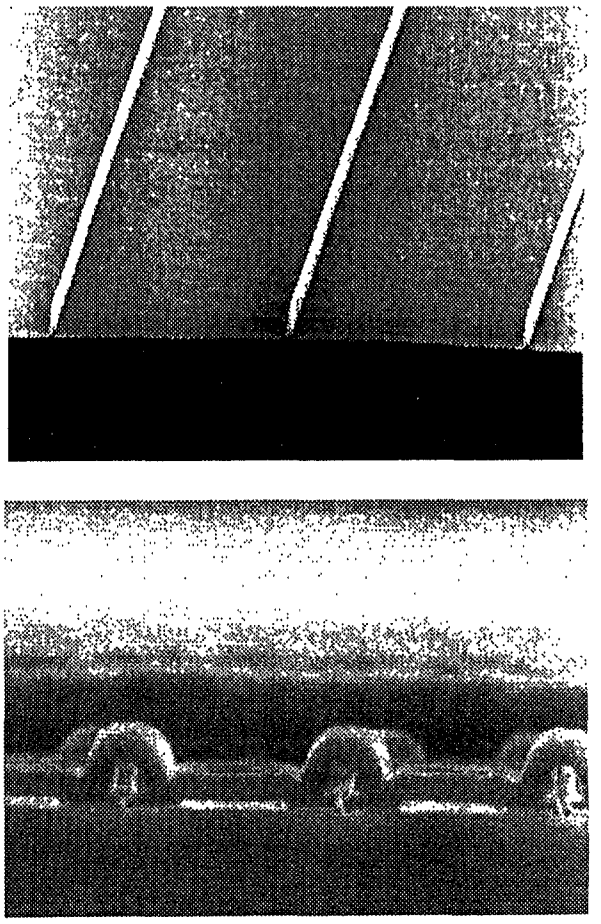

Fig.3 The fabricated dummy-gate by PEL method and multi finger gates.

The schematic cross-section of the IC is shown in Fig.4. The STO capacitors are fabricated by using the low-temperature sputtering process in order to avoid the deterioration of impurity profile of the epitaxial structure [6]. Thus obtained STO capacitor has the dielectric constant of 100 which is more than 15 times higher than that of conventional SiN one.

of 3.6 V and 3 mA, respectively, by the current-reuse configuration. Such low voltage operation can be achieved by 0.15 μm MODFETs fabricated by using the phase-shift lithography. Excellent high frequency performance such as CG of 30 dB, NF of 1.6 dB, and OIP3 of 9 dBm at 1.5 GHz is the inherent characteristics of deep submicron MODFET. The present GaAs front-end IC is suited for recent mobile communication systems including CDMA.

Acknowledgment

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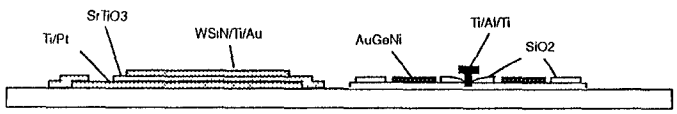

Fig.4 The schematic cross section of the present IC with 0.2μm gate MODFETs and STO capacitors.

Figure 5 shows the chip photograph of the present IC. The chip size is 1mm x 1mm. Owing to the STO capacitor technology, 200 pF of bypass and 80 pF of coupling capacitors were integrated in such small area.

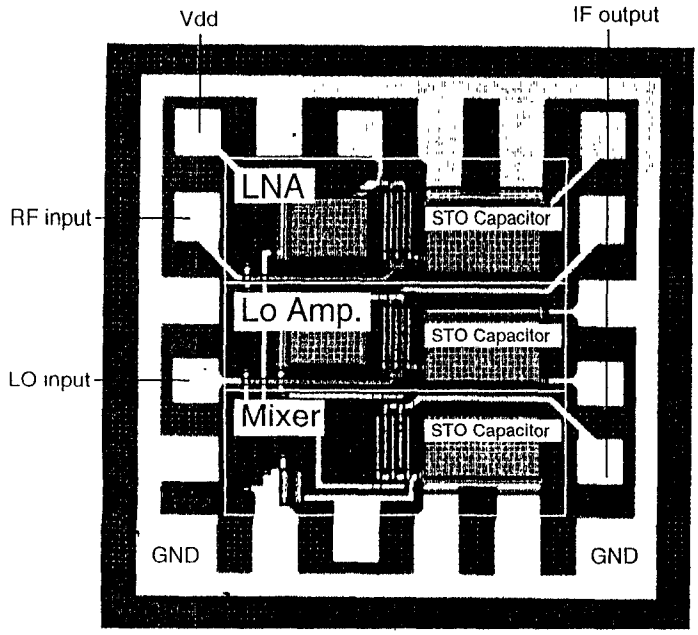

Fig.5 The chip photograph of the fabricated IC.

Measured Results

Figure 6 shows the gain and noise figure (NF) of the LNA as a function of applied voltage of the stage. The LNA with 0.15 μm gate FET exhibits highest gain and lower NF at the lowest operation voltage of 1V than those FETs with longer gate length. Figure 7 shows the input-output relationship of the whole IC at 1.5 GHz. As shown in the figure, the conversion gain (CG) and OIP3 (third-order output intercept point) are 30 dB and 9 dBm, respectively.

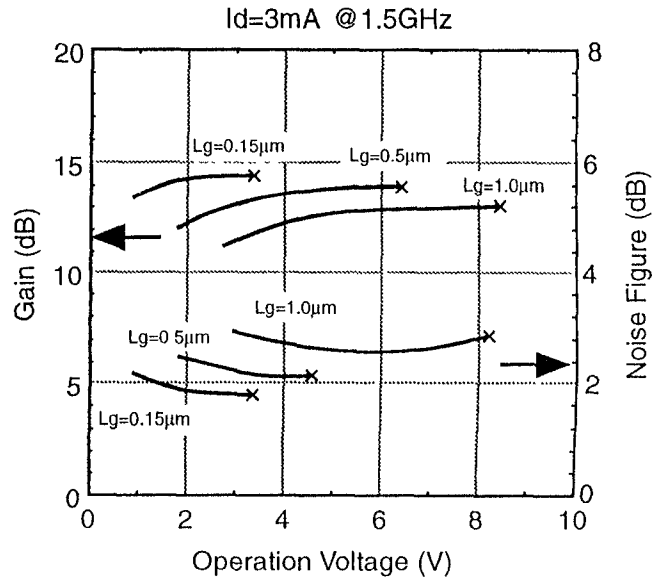

Fig.6 The gate length dependence of gain and noise figure of the LNA as a function of operation voltage.

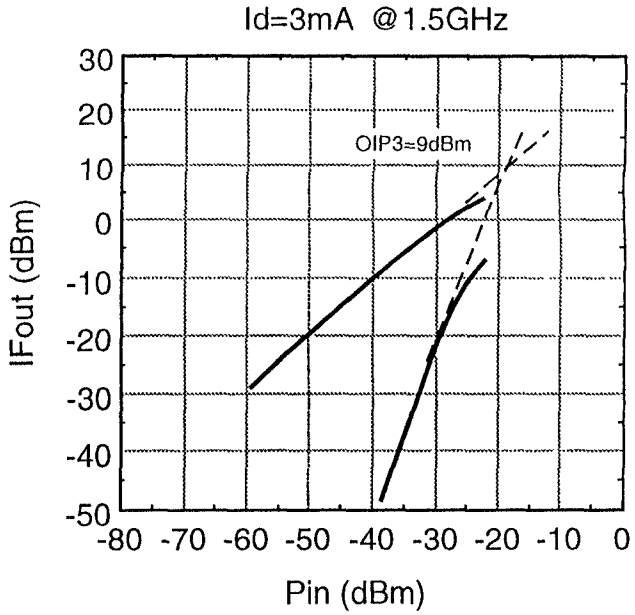

Fig.7 The performance of the fabricated IC with the current-reuse configuration.

Conclusion

We have developed a GaAs front-end IC that can operate at the condition of voltage and current